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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,362	UCHIDA ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-22* is/are allowed.

6)☒ Claim(s) *1-11,13 and 14* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11/23/01* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ancona (US 5,838,021) in view of Ohata et al. (US 5,963,471).

In re claim 1, Ancona shows (fig. 1) a logic circuit comprising a semiconductor substrate, a first single-electron device comprising a first conductive island (26) disposed over the semiconductor substrate at least two first tunnel barriers (12 and 14) disposed over the semiconductor substrate, the first conductive island being interposed between the first tunnel barriers, first and second electrodes (outputs right of junction 14 and input left of junction 12 respectively) disposed over the semiconductor substrate, the first conductive island being coupled with the first and second electrodes through the first tunnel barriers. A first charge storage region (capacitor 18) is insulatively disposed over the first conductive island. A second single-electron device has identical features of the first SED above and comprises a second conductive island (28) disposed over the semiconductor substrate, at least two second tunnel barriers (14 and 16) disposed over the semiconductor substrate, the second conductive island being interposed between the second tunnel barriers, third and fourth electrodes (input left of

barrier 14 and output right of barrier 16) disposed over the semiconductor substrate, the second conductive island being coupled with the third and fourth electrodes through the second tunnel barriers respectively, and a second charge storage region (20) disposed over the second conductive island, the third electrode of the second single electron device being connected to the first electrode of the first single-electron device (due to the common electrode at junction 14). Ancona does not specifically disclose the conductive islands and electrodes insulatively disposed on the substrate, so it is assumed that the device is formed on a bulk substrate. It is well known in the art that bulk substrate semiconductor devices can also be formed on silicon on insulator (SOI) substrates as well. However, Ohata et al. shows (fig. 15) an SED in which a conductive island (island Si), tunnel barriers, and electrodes (source and drain) are insulatively formed on substrate (Substrate Si). First and second SED's (200) and their components are disclosed in figure 28. Ohata et al discloses that SED's can be formed on SOI substrates as well as bulk substrates. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SED's formed on the bulk substrate of Ancona by insulatively forming them on SOI substrates because Ohata teaches that single electron devices on bulk substrates can be interchangeably formed on SOI substrates to insulate them from other semiconductor components in the device.

In re claim 2, Ohata discloses (col. 5, lines 52-58) which includes an output amplifier connected to the first electrode of the first single-electron device and the third

electrode of the second single-electron device (since the differential amplifier is connected to the outputs of each SET).

In re claim 3, Ancona shows (fig. 1) that the first and second single-electron devices include fifth (22) and sixth electrodes (24) insulatively disposed over the first and second charge storage regions, and logic signals are input of fifth and sixth electrodes of the first and second single-electron devices (22 and 24 are voltage sources). A logic operation result is output from the first and third electrodes (col. 6, lines 41-64).

In re claim 4, Ancona shows (fig. 1) that the first electrode and the third electrode are formed of a common electrode region (region at junction 14).

In re claim 5, Ancona shows (fig. 1) that the first and second single-electron devices include fifth (22) and sixth electrodes (24) insulatively disposed over the first and second charge storage regions, and logic signals are inputs of fifth and sixth electrodes of the first and second single-electron devices (22 and 24 are voltage sources). A logic operation result is output from the first and third electrodes (col. 6, lines 41-64).

In re claim 6, Ancona shows (fig. 1) that the first electrode and the third electrode are formed of a common electrode region (region at junction 14).

In re claim 7, Ancona discloses (col. 5, lines 1-17) wherein each of the first and second single-electron devices has logical inversion relation between a state that charges are accumulated in the charge storage region and state that no charge accumulated therein.

In re claims 8 and 9, Ancona shows (fig. 1) an element (22) configured to inject charges charge storage region or extract charges therefrom. The element (22) is also configured to generate a difference between the conductive island and the potential charge storage regions or to inject charges to the charge storage region or extract charges therefrom.

In re claims 13 and 14, Ancona shows (fig. 7) a logic apparatus includes a plurality of single-electron device pairs each including the first and second single-electron devices according to claim 1, the first and second single-electron device pairs being connected parallel and/or serial.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ancona (US 5,838,021) in view of Ohata et al. (US 5,963,471) as applied to claim 1 above, and further in view of Wasshuber .

In re claims 10 and 11, Ancona in view of Ohata et al. shows all of the elements of the claims except the Coulomb oscillation in the state the charges are accumulated in the charge storage region. Wasshuber discloses (col. 4, lines 3-15 and 45-65) SET in which a Coulomb oscillation in a state that charges accumulated in a charge storage region is shifted from that state so that no charge accumulated therein (this is done when writing a "1" or "0" in the storage region-1 denotes a charge accumulated and 0 denotes that no charge is accumulated). Wasshuber does not explicitly state that the shift is by a half period or that the size and materials of the conductive island are selectively set to shift the oscillation, but the SET of Wasshuber inherently shifts by

some period and the size and materials are inherently set to shift the oscillation because Wasshuber in combination with Ancona and Ohata discloses the same structure and materials and the Coulomb oscillation does perform the shift function. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the logic apparatus of Ancona and Ohata by shifting the state in which charges are stored or not stored by Coulomb oscillation as taught by Wasshuber to write and store data to a memory element.

Allowable Subject Matter

Claims 15-22 are allowed.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: the prior art references, alone or in combination, do not show a logic circuit comprising a first logic circuit using a first single electron device and having a capacitor, a second logic circuit using a second single electron device and having a capacitor, a first terminal connected to a first terminal of the first logic circuit, a resistor connected to a node of the first terminals of the first and second logic circuits and a voltage source, and a ground terminal connected to second terminals of the first and second logic circuits.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew E. Warren

December 19, 2003